

WHAT IS CLAIMED IS:

1. A semiconductor device comprising
a plurality of gate electrode structures formed on a semiconductor substrate,
5 each of which comprises:
a gate insulating film formed on said semiconductor substrate;
a gate electrode formed on said gate insulating film; and
an offset spacer formed on a side face of said gate electrode,
wherein respective lengths in said plurality of gate electrode structures are
10 substantially uniform with one another, each of said lengths being defined as a sum of a
gate length extending on an interface between said gate insulating film and said gate
electrode, and a width of said offset spacer extending on an interface between said offset
spacer and said semiconductor substrate.
- 15 2. The semiconductor device according to claim 1,
wherein said gate electrode includes a gate electrode having a rectangular
section, an upwardly tapered gate electrode and a downwardly tapered gate electrode
which are provided on the same semiconductor substrate.
- 20 3. The semiconductor device according to claim 3,
wherein a pair of shallow source/drain regions and a pair of deep source/drain
regions are formed to form a MOSFET, said regions in each of said pairs being formed in
said semiconductor substrate on opposite sides of a portion of said semiconductor
substrate immediately under said gate electrode.

4. A method of manufacturing a semiconductor device comprising the steps of:

(a) forming gate electrodes on a semiconductor substrate, each with a gate insulating film interposed therebetween;

5 (b) forming an insulating film on said gate electrodes by CVD;

(c) implanting an impurity into an entire surface of said insulating film;

(d) carrying out wet etching on said insulating film having said impurity implanted therein;

10 (e) carrying out anisotropic dry etching on said insulating film provided after said step (d), to form an offset spacer; and

(f) measuring a gate length of each of said gate electrodes after said step (a),

wherein said steps (b), (d) and (e) are modified based on a result of measurement provided by said step (f).

15 5. The method of manufacturing a semiconductor device according to claim 4,

wherein said insulating film is formed on said gate electrodes so as to have a thickness greater than a predetermined thickness in said step (b) when each of said gate electrodes is formed to have a gate length smaller than a predetermined gate length, and

20 said insulating film is formed on said gate electrodes so as to have a thickness smaller than said predetermined thickness in said step (b) when each of said gate electrodes is formed to have a gate length greater than said predetermined gate length.

6. The method of manufacturing a semiconductor device according to claim

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wherein said wet etching is carried out on said insulating film for a shorter time than a predetermined time in said step (d) when each of said gate electrodes is formed to have a gate length smaller than a predetermined gate length, and

5 said wet etching is carried out on said insulating film for a longer time than said predetermined time in said step (d) when each of said gate electrodes is formed to have a gate length greater than said predetermine gate length.